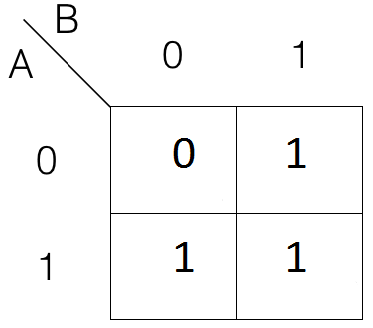
**DLD tasks**

**Q1) (a)**

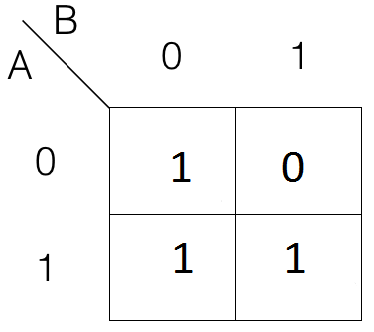
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| E | A | B | D0 | D1 | D2 | D3 |
| 1 | **X** | **X** | 1 | 1 | 1 | 1 |
| 0 | **0** | **0** | 0 | 1 | 1 | 1 |
| 0 | **0** | **1** | 1 | 0 | 1 | 1 |
| 0 | **1** | **0** | 1 | 1 | 0 | 1 |
| 0 | **1** | **1** | 1 | 1 | 1 | 0 |

**(b)**

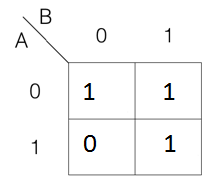
**D0:**

****

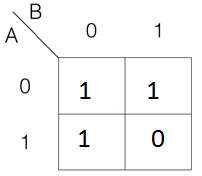
**D1:**

****

**D2:**

****

**D3:**

****

**SOP expressions:**

**D0 =** A+B

**D1 =** A+B’

**D2 =** A’+B

**D3 =** A’+B’

**POS expressions:**

**D0 =** AB

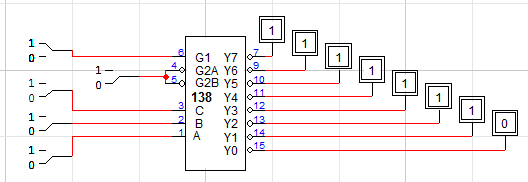
**D1 =** AB’

**D2 =** A’B

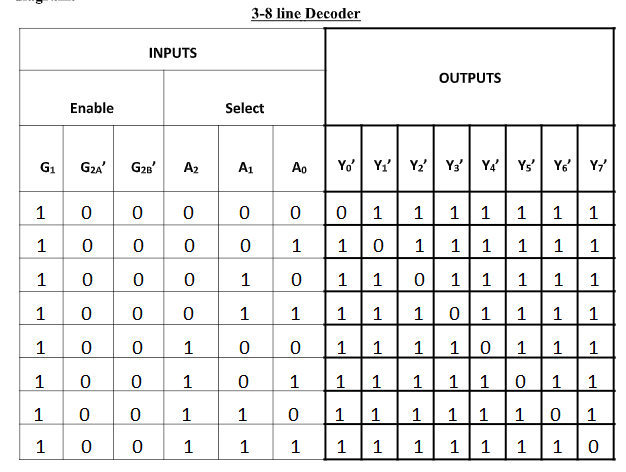
**D3 =** A’B’

**Q2)**

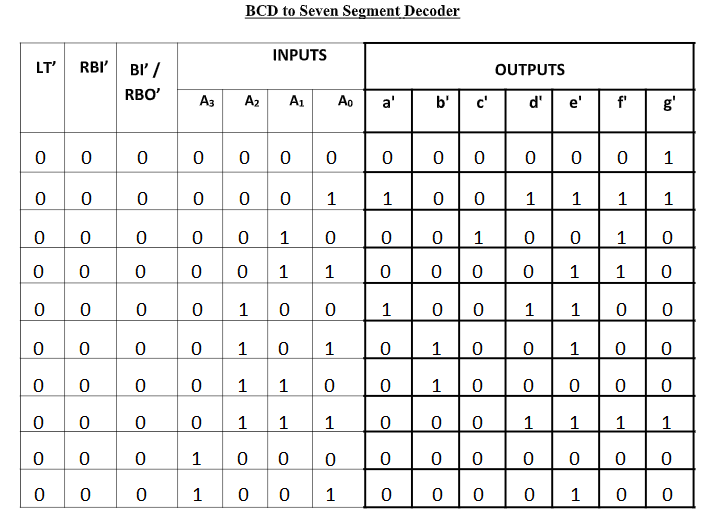
Circuit diagram:



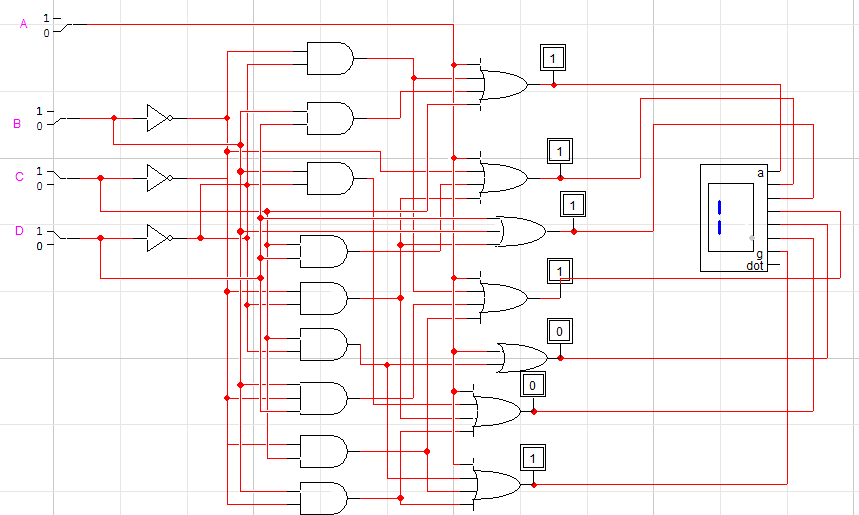
Truth table:



**Q3)**

****

**Q4)**

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